

NDD04N50Z

N-Channel Power MOSFET 500 V, 2.7 Ω

Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode–Protected Gate
- 100% Avalanche Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V _{DSS}	500	V
Continuous Drain Current R _{θJC}	I _D	3.0	A
Continuous Drain Current R _{θJC} , T _A = 100°C	I _D	1.9	A
Pulsed Drain Current, V _{GS} @ 10 V	I _{DM}	12	A
Power Dissipation R _{θJC}	P _D	61	W
Gate–to–Source Voltage	V _{GS}	±30	V
Single Pulse Avalanche Energy, I _D = 3.4 A	E _{AS}	120	mJ
ESD (HBM) (JEDEC22–A114)	V _{esd}	2800	V
Peak Diode Recovery	dv/dt	4.5 (Note 1)	V/ns
Continuous Source Current (Body Diode)	I _S	3.4	A
Maximum Temperature for Soldering Leads	T _L	260	°C
Operating Junction and Storage Temperature Range	T _J , T _{stg}	–55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

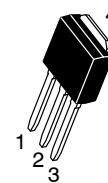
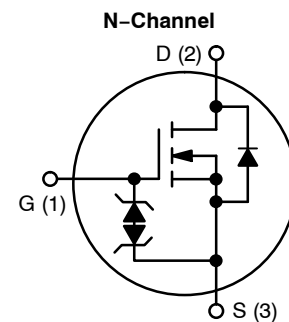
1. I_D ≤ 3.4 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C.



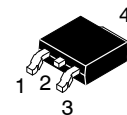
ON Semiconductor®

<http://onsemi.com>

V _{DSS}	R _{DS(on)} (MAX) @ 1.5 A
500 V	2.7 Ω



**IPAK
CASE 369D
STYLE 2**



**DPAK
CASE 369AA
STYLE 2**

MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NDD04N50Z

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.0	°C/W
Junction-to-Ambient Steady State	(Note 3) $R_{\theta JA}$ (Note 2) $R_{\theta JA-1}$	40 80	

2. Insertion mounted
3. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

Electrical Characteristics (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
----------------	--------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0 V, I_D = 1 mA$	500			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	Reference to 25°C, $I_D = 1 mA$		0.6		V/°C
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS} = 500 V, V_{GS} = 0 V$	25°C		1.0	μA
			150°C		50	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS} = \pm 20 V$			±10	μA

ON CHARACTERISTICS (Note 4)

Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10 V, I_D = 1.5 A$		2.3	2.7	Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 50 \mu A$	3.0		4.5	V
Forward Transconductance	g_{FS}	$V_{DS} = 15 V, I_D = 1.5 A$		2.1		S

DYNAMIC CHARACTERISTICS

Input Capacitance (Note 5)	C_{iss}	$V_{DS} = 25 V, V_{GS} = 0 V,$ $f = 1.0 MHz$	246	308	370	pF
Output Capacitance (Note 5)	C_{oss}		33	43	53	
Reverse Transfer Capacitance (Note 5)	C_{rss}		7.0	9.0	11	
Total Gate Charge (Note 5)	Q_g	$V_{DD} = 250 V, I_D = 3.4 A,$ $V_{GS} = 10 V$	6.0	12	18	nC
Gate-to-Source Charge (Note 5)	Q_{gs}		1.3	2.6	4.0	
Gate-to-Drain ("Miller") Charge (Note 5)	Q_{gd}		3.5	6.1	7.0	
Plateau Voltage	V_{GP}		6.6			V
Gate Resistance	R_g		1.8	5.4	16.2	Ω

RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250 V, I_D = 3.4 A,$ $V_{GS} = 10 V, R_G = 5 \Omega$		9.0		ns
Rise Time	t_r			9.0		
Turn-Off Delay Time	$t_{d(off)}$			16		
Fall Time	t_f			10		

SOURCE-DRAIN DIODE CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Diode Forward Voltage	V_{SD}	$I_S = 3.4 A, V_{GS} = 0 V$			1.6	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0 V, V_{DD} = 30 V$ $I_S = 3.4 A, di/dt = 100 A/\mu s$		240		ns
Reverse Recovery Charge	Q_{rr}			0.9		μC

4. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.
5. Guaranteed by design.

NDD04N50Z

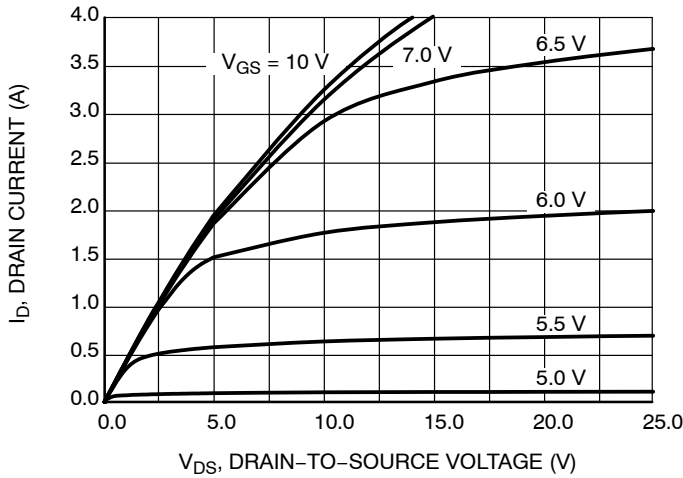


Figure 1. On-Region Characteristics

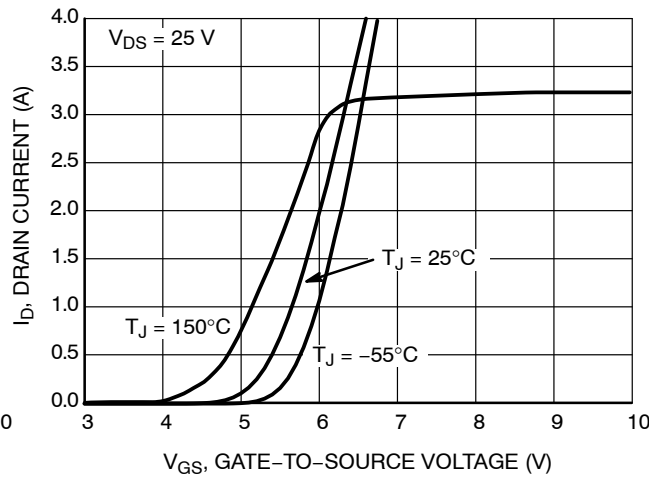


Figure 2. Transfer Characteristics

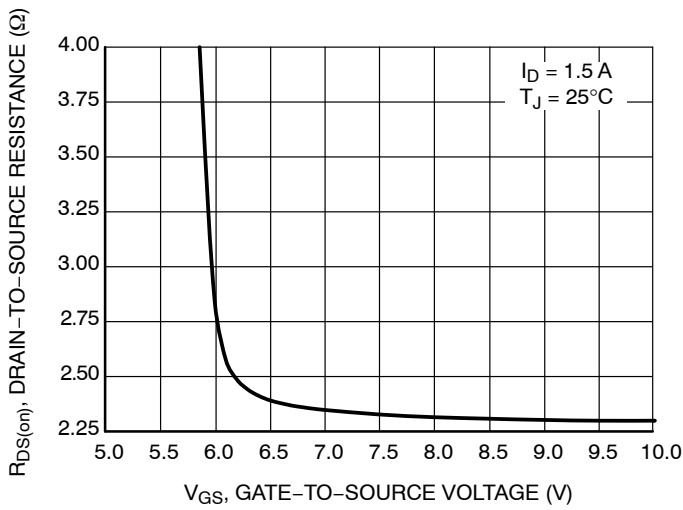


Figure 3. On-Region versus Gate-to-Source Voltage

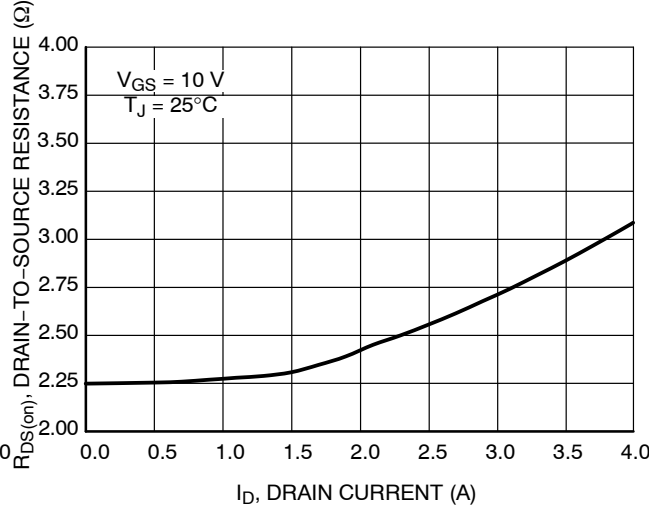


Figure 4. On-Resistance versus Drain Current and Gate Voltage

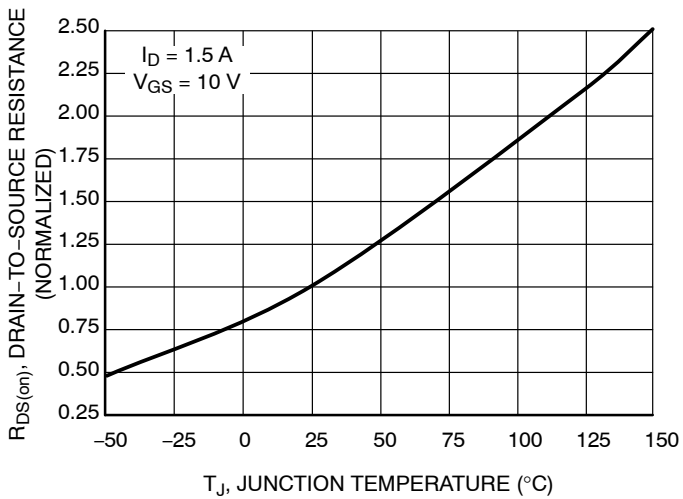


Figure 5. On-Resistance Variation with Temperature

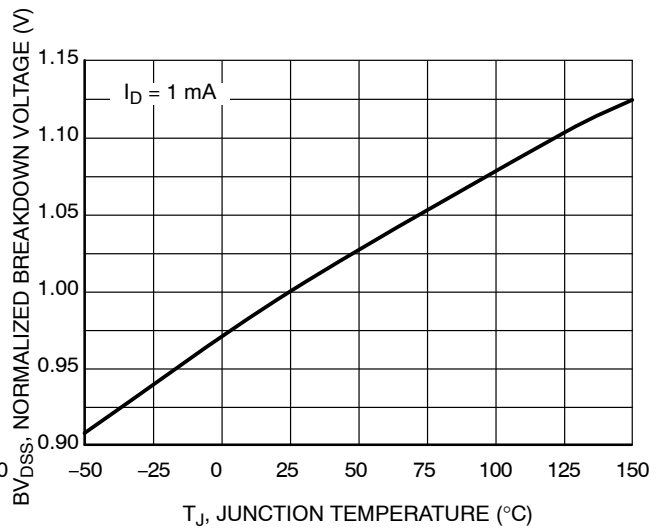


Figure 6. BV_{DSS} Variation with Temperature

NDD04N50Z

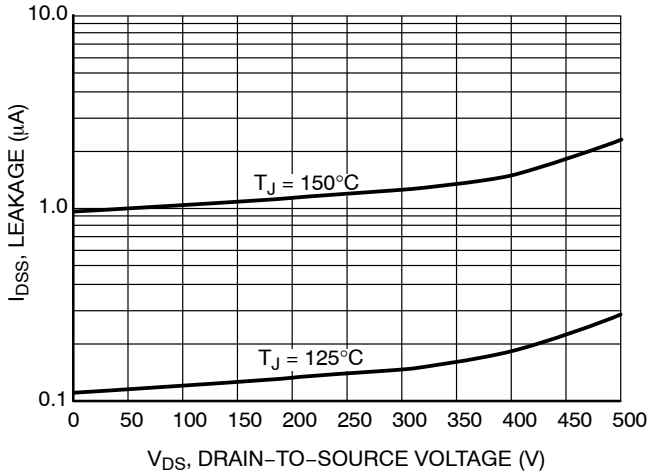


Figure 7. Drain-to-Source Leakage Current versus Voltage

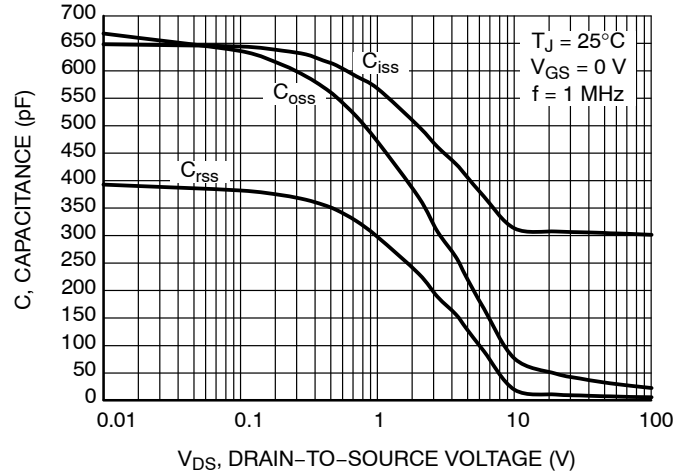


Figure 8. Capacitance Variation

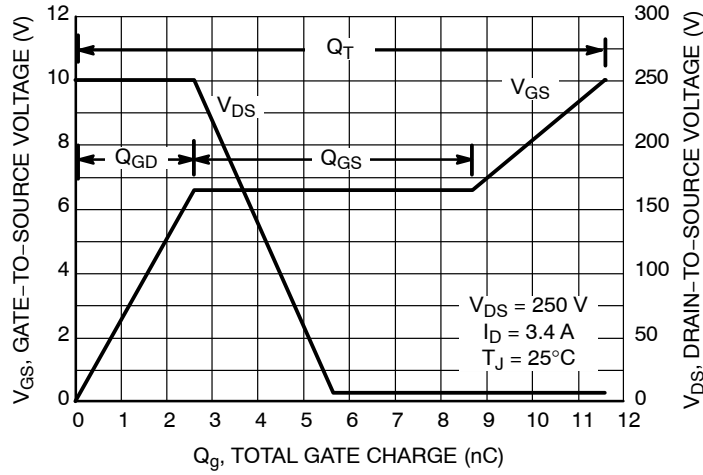


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

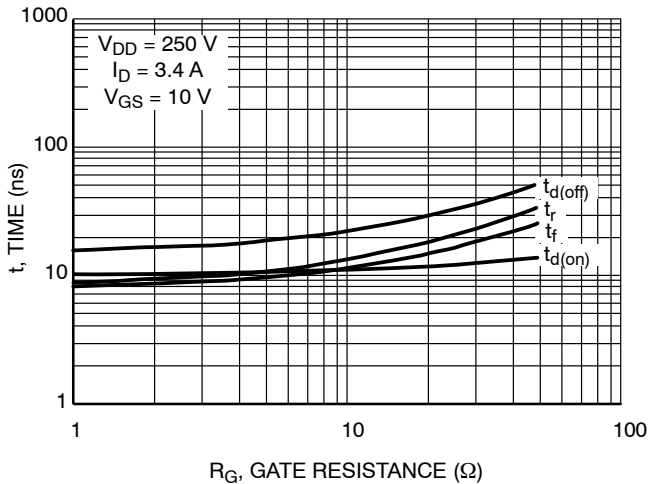


Figure 10. Resistive Switching Time Variation versus Gate Resistance

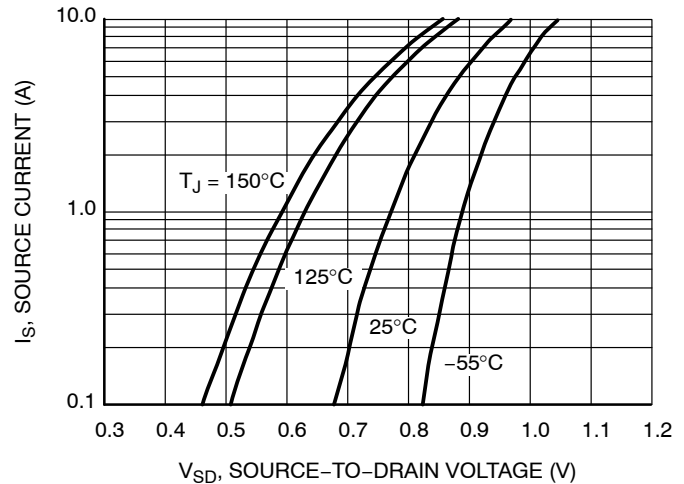


Figure 11. Diode Forward Voltage versus Current

NDD04N50Z

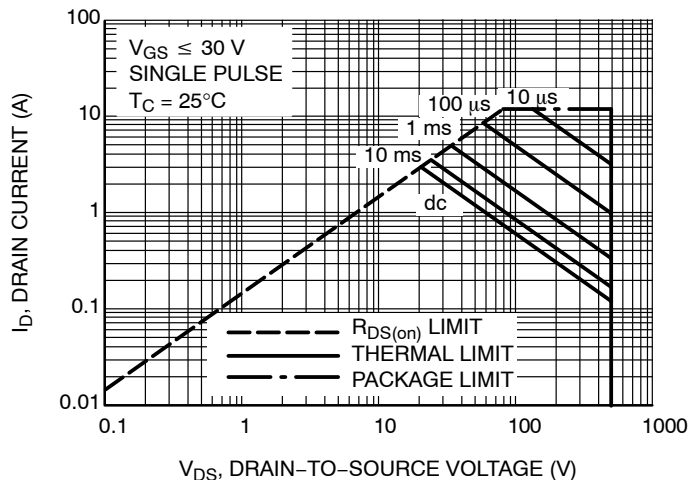


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDD04N50Z

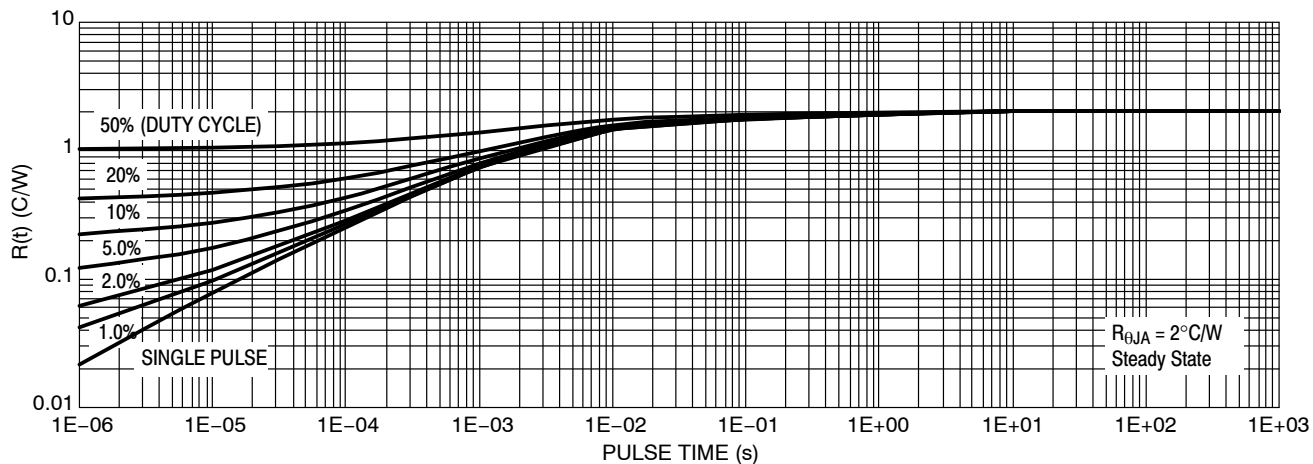


Figure 13. Thermal Impedance (Junction-to-Case) for NDD04N50Z

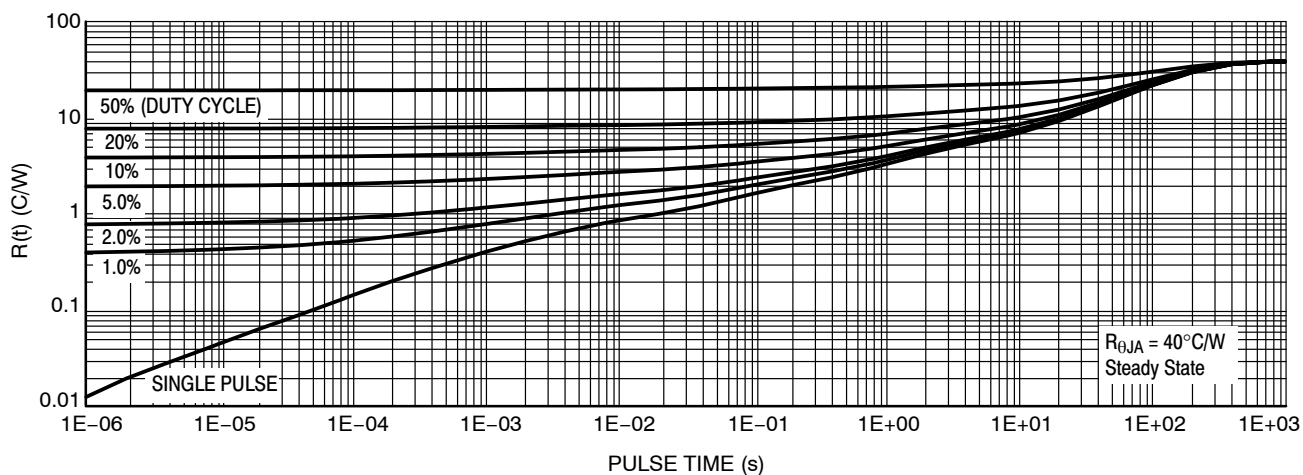


Figure 14. Thermal Impedance (Junction-to-Ambient) for NDD04N50Z

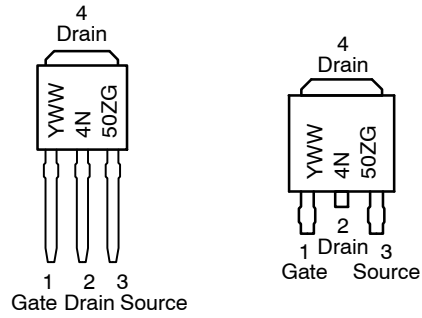
NDD04N50Z

ORDERING INFORMATION

Order Number	Package	Shipping†
NDD04N50Z-1G	IPAK (Pb-Free)	75 Units / Rail
NDD04N50ZT4G	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

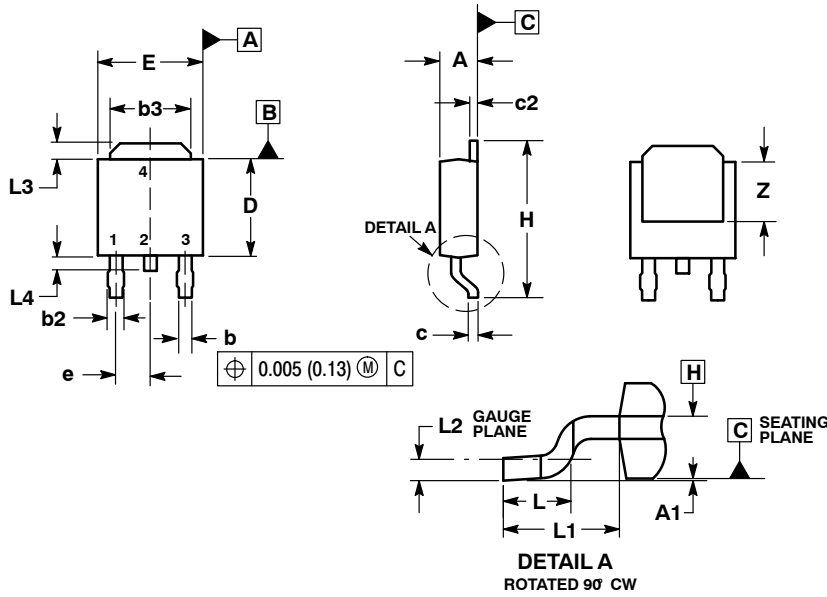


- A = Location Code
- Y = Year
- WW = Work Week
- G = Pb-Free Package

NDD04N50Z

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE) CASE 369AA-01 ISSUE B

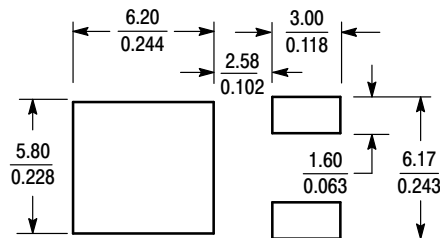


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 ($\frac{\text{mm}}{\text{inches}}$)

STYLE 2:

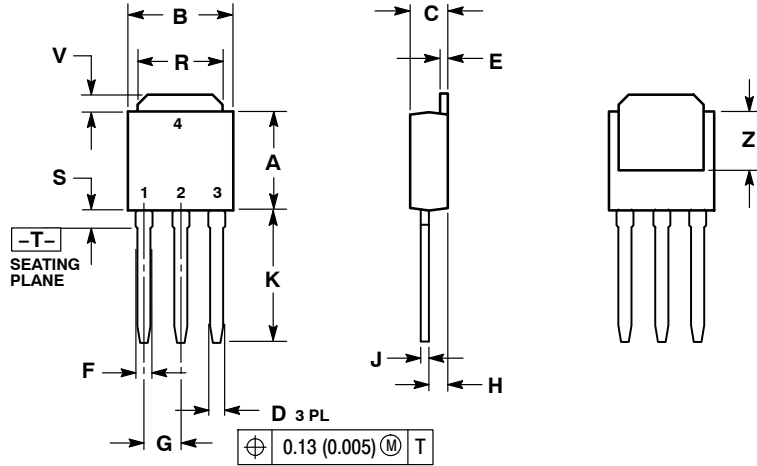
- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NDD04N50Z

PACKAGE DIMENSIONS

IPAK CASE 369D-01 ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
PIN 1: GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative